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A COMPUTATION ALGORITHM FOR ASSESSING VOLTAGE STABILITY AT AC/DC INTERCONNECTIONS

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Abstract: A new method for the analysis of ac voltage stability problems at HVDC terminals, when imbeded in large networks, is presented. The method can be used to evaluate the effects of dc modes of operation, ac system operating conditions and VAr compensation schemes on the combined system voltage stability. Dynamic properties of both ac and HVDC systems are incorporated in the solution algorithm. A step-by-step technique is developed for integrating the new algorithm with available load flow programs. Examples are given to demonstrate the performance of a new control strategy for HVDC converters connected to weak ac systems and the results are compared to classical solutions.

INTRODUCTION

With the rapid increase of HVDC utilization in the electric utility, for either transmission or for back-to-back applications, the relative portion of the dc power to the total system power is growing. In other words, ac systems at the terminals of HVDC schemes are becoming relatively weaker. This in fact constitutes a continuous challenge to the viability of HVDC in general and to its controllers in particular. Many serious problems in the overall performance of the combined ac/dc system can arise with consequences reflected on the total cost of the dc station. The one of particular interest, and highest in consequences, is the ac voltage stability at the HVDC terminals[1,2] It includes all operational problems related to ac voltage control under both steady state and dynamic conditions. To avoid this problem, additional ac equipment are usually employed at the dc terminals such as synchronous condensers and static VAr compensators. The cost of these devices, however, can offset the overall cost of the HVDC scheme and therefore may threaten its major economic advantage. This paper focuses on the fundamental frequency voltage stability aspect of the problem. In fact, this phenomena can be experienced at all HVDC converter terminals, whether in rectifier or inverter mode of operation, depending upon the ac system operating condition and the VAr compensation method.

To estimate the severity of such problems, available analytical techniques employ simplistic methods based upon the short circuit ratio (SCR) concept[2]. However, many practical factors, including control schemes and reactive power characteristics of the ac system, cannot be implemented in such techniques. Therefore, system planners tend to rely more heavily on the relatively expensive digital and physical simulation techniques in order to evaluate all possible alternative solutions.

This paper presents a new approach to provide system planners with a simple tool to effectively analyse the ac voltage control problem at the HVDC terminals before proceeding to other expensive and time consuming simulation techniques. The approach is based on small perturbation analysis of the combined ac/dc system. It allows for ac system voltage/VAr characteristics, impedances, generators and loads as well as HVDC modes of operation and VAr control schemes to be taken into account. Implementation of the algorithm in available utility digital programs enables users to study the problem for large ac networks containing multiple dc schemes.

ANALYTICAL APPROACH

On the subject of voltage stability and control at the HVDC terminals, the need has been recognized to provide the prospective user with a simple tool and guidance criteria to assess the viability of alternative solutions using HVDC in the early stages of planning.

The proposed analytical approach is meant to fill the gap between simplistic approaches, using the SCR criteria, for preliminary judgement and carrying out detailed studies by means of digital and analogue simulations. Although other techniques have been proposed in the past[3-4]; yet they have not gained a wide acceptance either because they are not realistic or involve many parameters unknown to the system planner. Therefore, the attempt is made here to simplify, as possible, the modelling method as well as the solution algorithm when realistic characteristics are considered. The new algorithm allows a modular representation of individual system components. Therefore, available utility digital programs for ac system analysis, such as load flow, can be utilized.

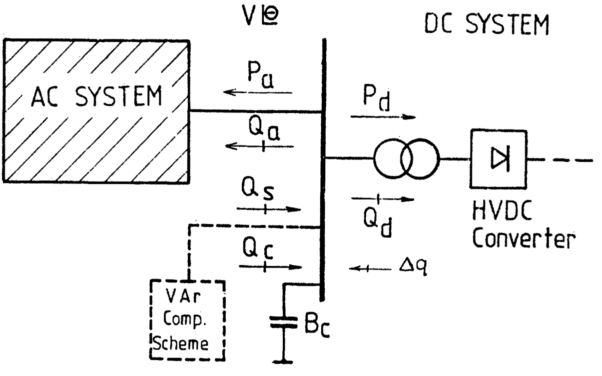

Fig. 1 Major system components at ac/dc junction

Fig. 1 depicts typical system components present at each ac/dc interconnecting point. The power Pd into the HVDC converter is positive when in rectifier and negative when in inverter operation. The reactive power Qd consumed by the converter and measured at the ac terminal of the converter transformer is always positive as shown in Fig. 1. Qa represents the VAr required by the ac network to maintain a particular scheduled voltage V

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at the HVDC terminal. This reactive power should be determined since it can have a considerable impact on the voltage stability of the combined ac/dc system. To supply both Qd and Qa, VAr compensation schemes are often needed. A part of the VAr requirements is supplied by the ac filters and shunt capacitors installed at the terminal. These are represented as succeptance Bc at the fundamental frequency.

The proposed method for evaluating voltage stability, does not rely on simultaneous solution of the ac system and the HVDC or VAr compensation schemes. Therefore, after a normal ac load flow solution is obtained, with few additions to the LF program, factors for voltage stability are computed. The effects of various dc modes of operation and alternative methods for voltage control can then be assessed with no load flow iterations.

VOLTAGE STABILITY CRITERIA

The phenomena of voltage stability, at system fundamental frequency, exclude all other types of stabilities such as harmonic and phase angle, or transient stabilities. It can, however, be related to the magnitude of ac voltage excursions during steady state and dynamic conditions. Similar to the well known voltage stability phenomena associated with ac transmission, with different loadings at different power factors, the ac voltage stability at an HVDC terminal may be defined. However, because of the complex relationships between the dc converter performance, the VAr compensation schemes and the ac system, it is more convenient to study analytically the small signal behavior of the combined system. In this line of thought, a good measure for ac voltage stability could be the per-unit incremental change of ac voltage due to a change ' q' in the infeed reactive power supply at the HVDC terminal. In mathematical terms, this can be defined as "Voltage Stability Factor" at a specific dc power transfer:

$$\mathrm{VSF} = (\Delta V/V)/\,\Delta q\,\Big|_{Pd} \tag{1}$$

Similar to ac line voltage stability, VSF is positive for a stable system and is negative when the system is suffering from voltage instability. However, the excursions in voltage magnitude would be proportional to the VSF. High values of VSF, therefore, indicate that the system will show high voltage fluctuations when subjected to transients, e.g. high temporary overvoltages for high positive VSF.

COMPUTATION TECHNIQUE

From the definition made in Eq. 1 it may appear that calculation of the VSF would be sufficient by means of successive load flow runs. However, such an approach will overlook the inherent dynamic properties of either ac or dc systems. Once the main dynamic characteristics are considered in the analysis, resulting VSF can be closely correlated to system behavior under all steady and dynamic conditions. For this purpose, incremental changes of all system variables are calculated individually by linearizing the system relationships around each operating point. The VSF is computed by eliminating all dependent variables. This approach is different from the eigenvalue technique which is concerned about control and phase angle stabilities.

Recently,[5] the VSF has been calculated for an isolated dc terminal connected to an equivalent ac system. The general procedure described here, however, can be applied to study multiple dc schemes simultaneously connected to large ac systems. Using the notations of Fig. 1, the incremental reactive power balance at each ac/dc interconnection is :

$$\Delta q = \Delta Qa + \Delta Qd - \Delta Qc - \Delta Qs \tag{2}$$

Therefore;

$$\mathrm{VSF} = \frac{1}{(\frac{\Delta Qa}{\Delta V/V}) + (\frac{\Delta Qd}{\Delta V/V}) - (\frac{\Delta Qc}{\Delta V/V}) - (\frac{\Delta Qs}{\Delta V/V})}\Bigg|_{Pd} \tag{3}$$

Each element in the denominator of Eq. 3 represents the incremental Q/V characteristics of the particular system component at the power transfer level Pd. These elements will be computed individually.

Incremental Q/V Characteristics of AC System

The incremental VAr injection Δq, shown in Fig. 1, will cause a change in the voltage $V\angle\theta$ at the interconnecting point 'i'. From the basic load flow relationships, the incremental changes ΔV and $\Delta\theta$ are related to the rest of the network by:

$$\begin{aligned}
\frac{\partial Pa}{\partial \theta}\Delta\theta + \frac{\partial Pa}{\partial V}\frac{\Delta V}{V} &= -\sum_{k\neq i}\frac{\partial Pa}{\partial \theta k}\Delta\theta k - \sum_{k\neq i}\frac{\partial Pa}{\partial Vk}\frac{\Delta Vk}{Vk}\\
\frac{\partial Qa}{\partial \theta}\Delta\theta + \frac{\partial Qa}{\partial V}\frac{\Delta V}{V} &= -\sum_{k\neq i}\frac{\partial Qa}{\partial \theta k}\Delta\theta k - \sum_{k\neq i}\frac{\partial Qa}{\partial Vk}\frac{\Delta Vk}{Vk} + \Delta Qa
\end{aligned} \tag{4}$$

assuming no change in power Pa.

Eq. 4 represents the ac system Jacobian J with all injections in P and Q set to zero except ΔQa.[6] If matrix M denotes the inverse of the Jacobian (J^{-1}) we get:

$$\begin{bmatrix} \Delta\theta \\ \Delta\theta k \\ \cdots \\ \Delta V/V \\ \Delta Vk/Vk \\ \cdots \end{bmatrix} = \left[\begin{array}{c|c} M_1 & M_2 \\ \hline M_3 & M_4 \end{array}\right] \begin{bmatrix} 0 \\ 0 \\ \cdot\cdot \\ \Delta Qa \\ 0 \\ \cdot\cdot \end{bmatrix} \tag{5}$$

Therefore;

$$\frac{\Delta Qa}{\Delta V/V} = 1/m_4(i,i) \tag{6}$$

where, $m_4(i,i)$ is the diagonal element in the inverse Jacobian matrix M which corresponds to the ac/dc junction bus (i).

Computation of the matrix J is well known[6]. In fact, available load flow programs form the Jacobian and its inverse, in a sparse form, as part of Newton method. However, J as computed from a load flow has to be modified to reflect the ac system dynamics. A simple approach would be to model all generators and loads as a combination of current source and impedance models. This is similar to the modeling used in standard stability programs.[7]

Incremental Q/V Characteristics of HVDC Terminals

For each HVDC converter terminal, the basic steady state equations (Appendix I) are linearized in the form:

$$A.\,\Delta y = b.\,\Delta u \tag{7}$$

where;

$$A = \begin{bmatrix} -1 & -Rc & 0 & VT\cos & VT \\ Id & Vd & 0 & 0 & 0 \\ 0 & 0 & Pd(VT/Vd)^2 & 0 & 0 \\ -1 & 0 & -Qd/Id & Vd & 0 \end{bmatrix} \tag{8}$$

$$\Delta y = \begin{bmatrix} \Delta Vd \\ \Delta Id \\ \Delta\phi \\ \Delta V/V \\ \Delta\cos\alpha \end{bmatrix},\quad b = \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ -Qd/Pd & 1 \\ 0 & 0 \end{bmatrix},\quad \Delta u = \begin{bmatrix} \Delta Pd \\ \Delta Qd \end{bmatrix} \tag{9}$$

An equation representing the particular converter controller is also required. It may represent the linearized characteristics of constant current or constant extinction angle control modes or any other controller for voltage or reactive power control. For practical cases, it is sufficient to model such a control system by a simple PI-function. In this case only the gain and slope will appear in the linearized equation. For constant γ control, however, we have:

$$(2Rc/VT)\Delta Id - (2Rc\ Id/VT)\Delta V/V - \Delta\cos\alpha = \Delta\cos\gamma \qquad (10)$$

Because of the fast γmin controller, $\Delta\cos\gamma = 0$.

When more than one HVDC terminal need to be simultaneously studied, a linearized equation relating Vd and Id of all terminals is added. The resulting equations can then be rewritten in the form:

$$A'' . \Delta y = b'' . \Delta u \qquad (11)$$

Hence, $$\Delta y = A''^{-1} . b'' . \Delta u \qquad (12)$$

Assuming that no change in dc power Pd takes place, therefore;

$$\Delta Qd/(\Delta V/V) = 1/c''_{(4)} \qquad (13)$$

where, $c''_{(4)}$ is the element no. 4 of $[A''^{-1}.b'']$

IMPLEMENTATION IN LOAD FLOW PROGRAM

As mentioned before, ac system VAr requirements have to be established. Therefore, load flow studies are a must. The ac voltage at each ac/dc junction bus is fixed while the amount of the dc power infeed is varied, i.e. PV-bus representation with open Q-limits. The VAr absorbed by the dc terminal is assumed to be fully compensated. Resulting Qgen at these PV-nodes represent the reactive power demand Qa of the ac system.

Different scheduled voltages, load scenarios, network contingencies and generation scheduling have to be studied in order to obtain a complete picture of the ac system VAr characteristics.

Following every load flow solution run, the voltage stability factor at each HVDC terminal (i) can be calculated as follows:

Step 1. Model bus (i) as PQ-model.

Step 2. Replace all generators by their current source model. As a good approximation, generator Xd' can be added to the self admittance of its terminal bus.

Step 3. Change all loads to stability model, i.e. combinations of constant Z, I and P.

Step 4. Construct the ac system Jacobian matrix. In case that the LF program uses Newton method, implement the above modifications directly in the factorized J matrix.

Step 5. Set all mismatches in P & Q to zero except Qa(i) = 1.

Step 6. Compute the diagonal element $m_4(i,i)$ of the inverted J matrix. Use Eq. 6 for calculating $\Delta Qa/(\Delta V/V)$.

Step 7. Construct HVDC system matrix A" from Eq. 11 and use Eq. 10 for calculating $\Delta Qd/(\Delta V/V)$.

Step 8. For shunt capacitors and filters installed at bus (i);

$$\Delta Qc/(\Delta V/V) = 2V^2Bc \qquad (14)$$

Step 9. Calculate the Voltage Stability Factor (VSF) using Eq. 3.

VOLTAGE STABILITY WITH CONVENTIONAL CONTROLS

HVDC converters, whether in inverter or rectifier mode of operation, for either long distance transmission or back-to-back applications are liable to voltage stability problems when controlled by conventional methods. Of course the characteristics and impedance of the connected ac system play a major role in displaying and enhancing such problems.

Fig. 2(a) shows the VSF for an inverter terminal connected to ac system with SCR=2.37. The inverter is assumed to be operating at constant γ min in all range of dc power transfer. The reactive power support from the ac network, excluding any VAr compensartion, to maintain a 1.0 pu voltage at the ac bus is shown in Fig. 3(a). All values are expressed in pu based on nominal Pd.

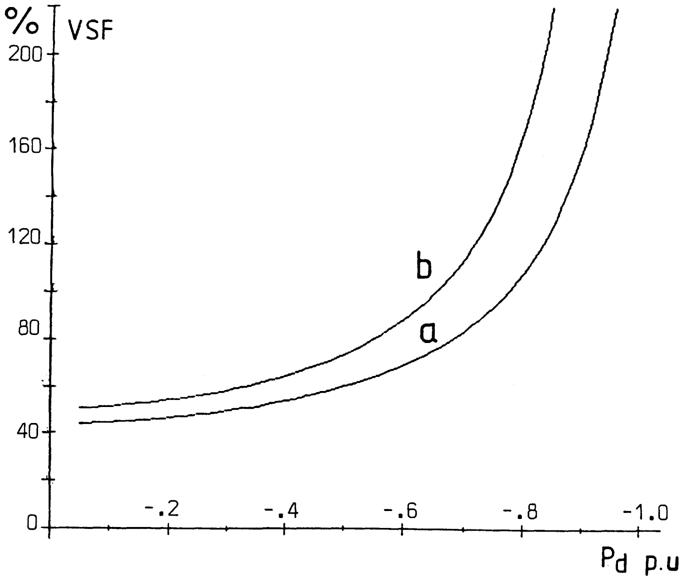

Fig. 2 Voltage Stability Factor for inverter with γmin control. SCR= 2.37
(a) for Qa characteristics of Fig. 3(a)
(b) for Qa characteristics of Fig. 3(b)

When the ac system has a different Qa requirements, as shown by curve (b) in Fig. 3, but with the same SCR, the VSF changes as shown in Fig. 2(b). The slight aggrevation in voltage stability in the latter case is because Qa is more inductive. Therefore, the VAr compensation scheme would be more capacitive. However, when the ac system impedance is changed such that SCR =1.8, the VSF shows more instability as depicted by Fig.4(a).

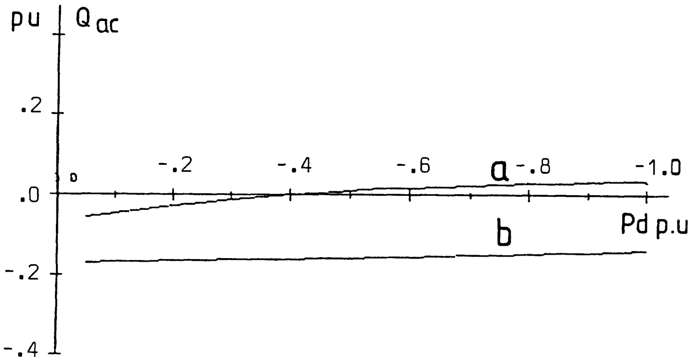

Fig. 3 AC system reactive power characteristics

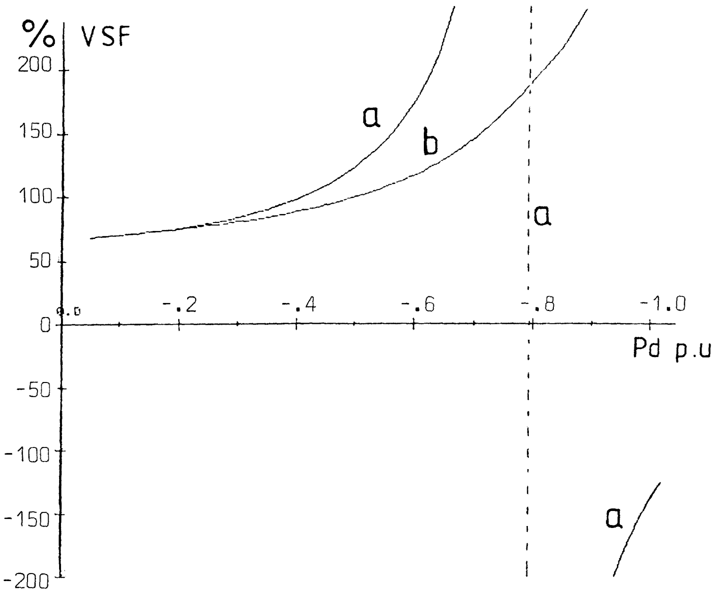

Fig. 4 Voltage Stability Factor for inverter. SCR=1.8
(a) constant γ control
(b) constant β control

One reason for such voltage instabilities is because operation with constant extinction angle has inherent negative characteristics. Such characteristics can be depicted by the negative $\Delta Qd/\Delta V$ shown in Fig. 5(a).

Attempting to operate the inverter with constant β (or equivalently constant α) would improve the voltage stability as shown in Fig. 4(b). Note the similarity of the VSF in Figs. 4(b) & 2(b). The effect of constant β compared to γmin control, in this case, is almost equivalent to increasing the SCR by 0.5. The reason behind this improvement is that the $\Delta Qd/\Delta V$ behavior of the inverter with β control is positive (Fig. 5b). This positive characteristic is, however, not sufficiently large enough to counteract the destabilizing effect of the ac system in this case.

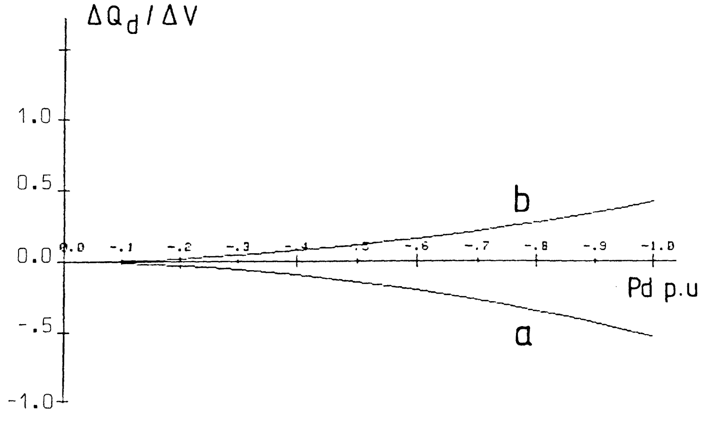

Fig. 5 Incremental Qd/V characteristics for inverter
(a) constant γ control
(b) constant β control

VOLTAGE STABILITY WITH VAr COMPENSATION SCHEMES

Synchronous and static reactive power compensators are the classical solutions for VAr compensation and voltage control at HVDC terminals when suffering from voltage stability problems[8]. To include these devices in the above analysis, few additions are required.

Synchronous Condensers

A synchronous condenser is often modeled by a voltage source Esy with an angle δsy behind a transient reactance Xsy. Incremental power balance equations at the dc terminal are accordingly modified. These can be directly implemented in Eqs. 7 & 8.

For Q-balance (row 3 in A-matrix) add:

$$-\ (\ Qsy\ -V^2/\ Xsy\ ).\ \Delta V/V \qquad (15)$$

and for P-balance (row 2 in A-matrix) add :

$$-(\ Qsy\ +\ V^2/\ Xsy\ ).\ \Delta\delta sy \qquad (16)$$

where, Qsy is the reactive power supplied by the syn. condenser and Xsy = Xd' + X (step-up transformer). In this case another linear equation representing the small signal effect of synchronous condenser field and excitation system is added to the A"-matrix of Eq. 11.

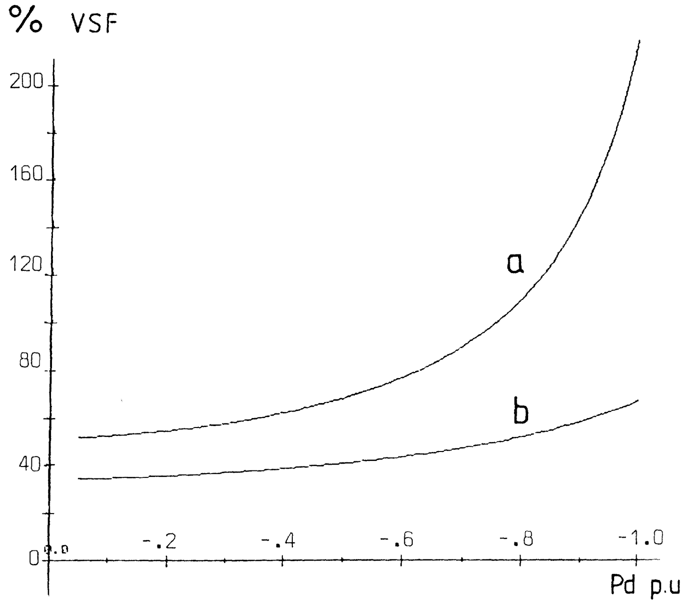

Fig. 6 VSF for inverter with γmin control. SCR= 1.8
(a) with synchronous condenser of 25% rating
(b) with synchronous condenser of 50% rating

The system studied earlier, where an HVDC inverter is operating with γ min control and the SCR=1.8, is now examined. With a rating of 25% the synchronous condenser can eliminate the possibility of voltage instability but with a poor voltage regulation as seen by comparing Fig. 6(a) to Fig. 4(a). To be effective in voltage control, the compensator should have a higher rating, say 50% (Fig. 6b).

Static VAr Compensators

Static VAr compensation (SVC) schemes are usually a mixture of thyristor switched capacitors (TSC), thyristor controlled reactors (TCR), fixed capacitors and reactors The rating of each component in the VAr compensating scheme is determined by the VAr requirements at the ac/dc interconnecting point. However, other economic factors may influence the choice of the minimum unit rating.

To implement this type of VAr compensation in the computation of voltage stability at the HVDC terminals two models are employed: Fixed shunt succeptance (Bs) and controlled VAr source (Qs) models.

Fixed capacitors and reactors are represented by the Bs model. Also, since the TSC are physically switched in discrete steps they can be represented by the Bs model as well but only for the "switched-on" banks. To include this model in the A-matrix of Eq.8, add to row 3:

$$-(2\,V^2\,Bs).\,\Delta V/V \qquad (17)$$

where Bs is positive for capacitive VAr's and equals to: net rating/Vn^2 for all switched-on banks.

On the other hand, a TCR can be represented by its external V/I characteristics including its step-up transformer. In this case row 3 in A-matrix is modified by:

$$+\,(Qs + Ks\,V^2).\,\Delta V/V \qquad (18)$$

where, $Ks = Qsn\ (pu)/slope \qquad (19)$

and the slope is defined in terms of the nominal controlled range Qsn of the TCR. When the TCR is operating outside the controlled range, then :

$$Ks = 1/Xst \qquad (20)$$

and the model is automatically transformed to the Bs model since;

$$Xst = Vn^2 \,/\, Qsn\ (pu) \qquad (21)$$

For the same studied inverter system with SCR=1.8, a SVC scheme with a 50% TCR and a fixed capacitor is employed instead of synchronous condensers. The VSF is highly improved as shown in Fig. 7 (a).

The reason for the effective voltage control in this case is that the TCR is able to react, in a fast manner, to any voltage variations at the ac/dc junction. This is reflected by the combined SVC+HVDC incremental Q/V characteristics shown in Fig. 8 (a). Note the order of magnitude of such a ratio compared to Fig. 5.

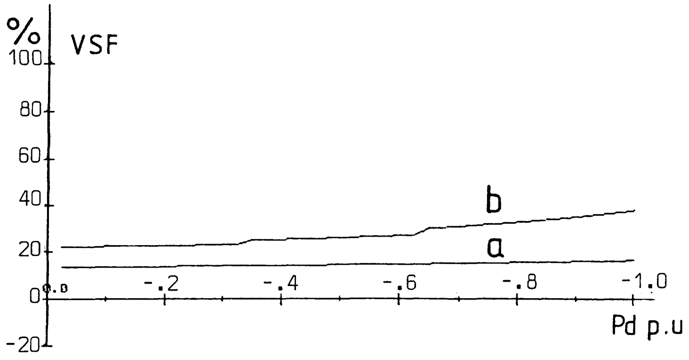

Fig. 7 VSF for inverter with γmin control. SCR= 1.8
(a) with static VAr comp. : TCR 50% rating
(b) with static VAr comp. : TCR 25% rating

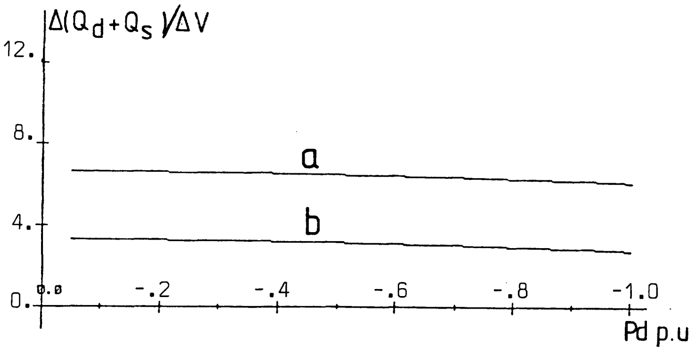

Fig. 8 HVDC+SVC incremental Q/V characteristics for inverter with γmin control
(a) TCR of 50% rating
(b) TCR of 25% rating

If a SVC scheme is chosen with a smaller rating of 25% TCR but with two 15% switched capacitor banks, the VSF is slightly degraded as shown in Fig. 7 (b). The operation for such a scheme would be as shown in Fig. 9 .

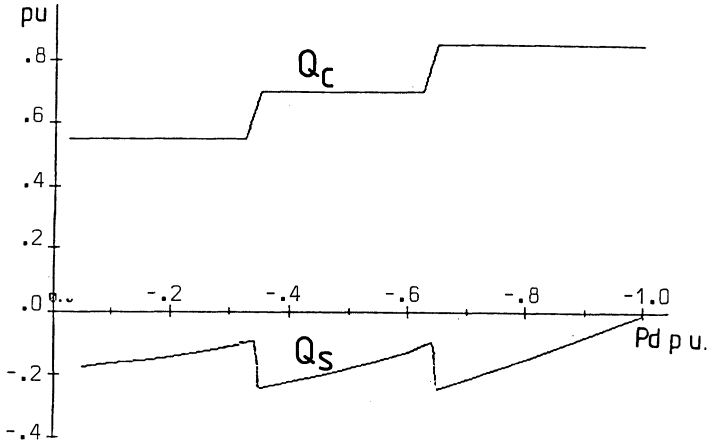

Fig. 9 Reactive power supply by fixed and switched capacitors (Qc) and TCR (Qs)

VOLTAGE STABILITY WITH NEW HVDC CONTROL TECHNIQUES

Recently introduced advanced converter control techniques, utilizing micro-processors, have realized a greater flexibility and economic operation of HVDC schemes.[8-10] By extending the basic characteristics and nominal operating domain of HVDC converters, it is now possible to affect and modulate the reactive power balance, on a continuous and temporary basis, at the ac/dc junction points. By making full utilization of the dc converter valves, no external VAr control equipment would be required.

By such techniques,[8] the HVDC converters change their reactive power absorption according to the steady state VAr requirements of their interconnected ac systems. This is realized by local controllers at the dc terminals. Switched capacitor and reactor units at each terminal are coordinated to provide the necessary Q-bias. The continuous regulation of Qd produces a smoothing effect at the instants of switching as shown in Fig 10. Coordination among the dc terminals may be necessary, but in a slow manner, in order to minimize the overall system losses during steady state conditions.

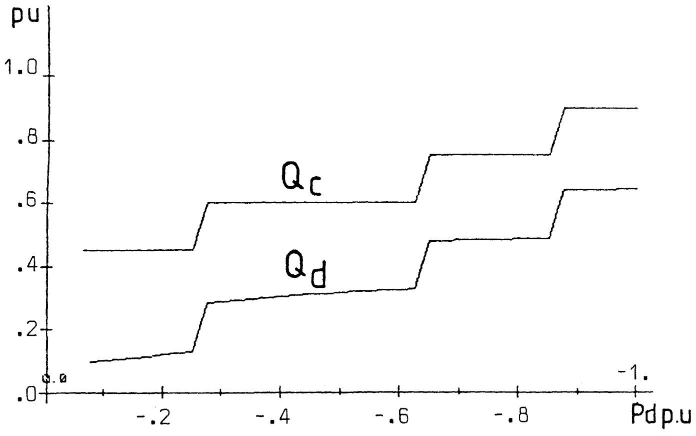

Fig. 10 Reactive power coordination with new HVDC control technique

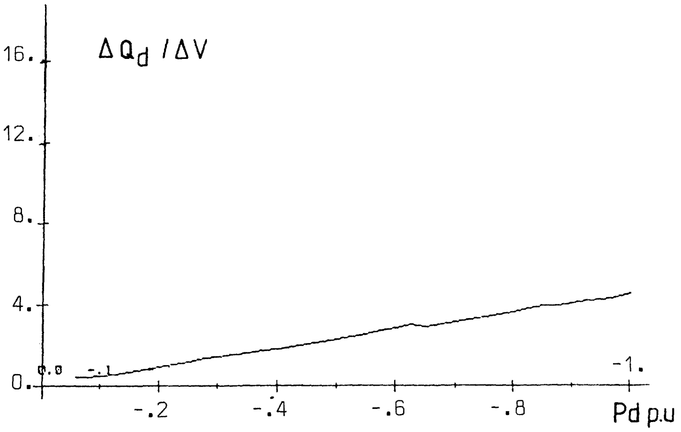

Fig.12 Incremental Qd/V characteristics for inverter with new controls

During transient conditions, however, when the ac voltage adjacent to a HVDC terminal experiences unacceptable variations, an immediate control action will be exercised to alter the reactive power absorbed by the dc converter. Thus limiting such voltage excursions. This is achieved by temporarily changing the dc voltage, through firing (or extinction) angle, by means of the fast converter controllers.

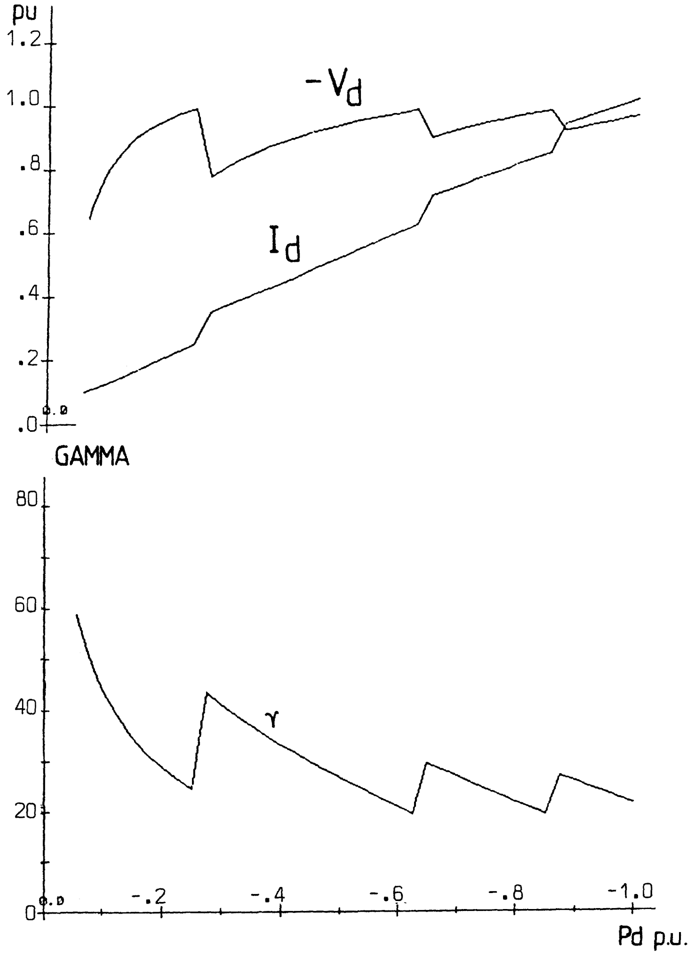

Fig.11 Inverter steady state operation with new controls

Applying this technique to the HVDC system discussed before, produces the steady state variations of the inverter variables shown in Fig. 11. Coordination with switched capacitors are necessary in this case to keep the operating dc voltage close to nominal value. Due to this new control technique, the incremental Q/V characteristics of the inverter terminal is highly improved as depicted by Fig. 12. The resulting voltage stability factor for the combined ac/dc system is shown in Fig. 13. Comparing the VSF with the new control technique to other methods of compensation reveals the superiority of such technique in improving the voltage stability at the HVDC terminal.

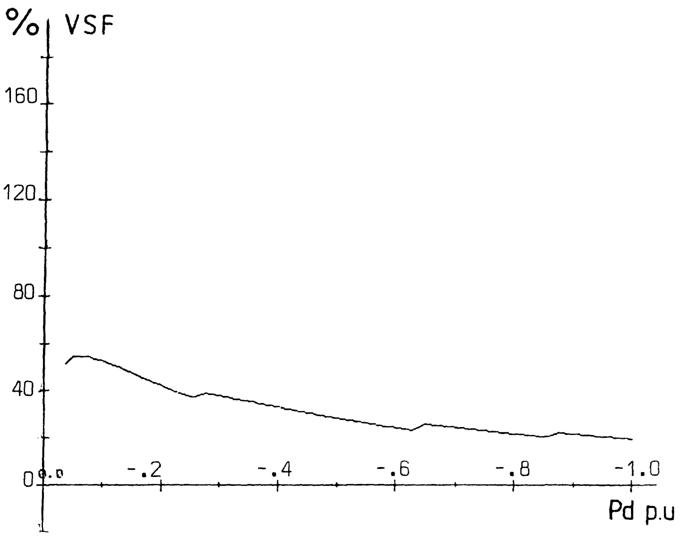

Fig.13 Voltage Stability Factor for inverter with new controls. SCR= 1.8

Correlation to Transient Performance

Fig. 14 shows the time simulations for the same ac/dc system, with and without the new control method, following a severe ac fault.

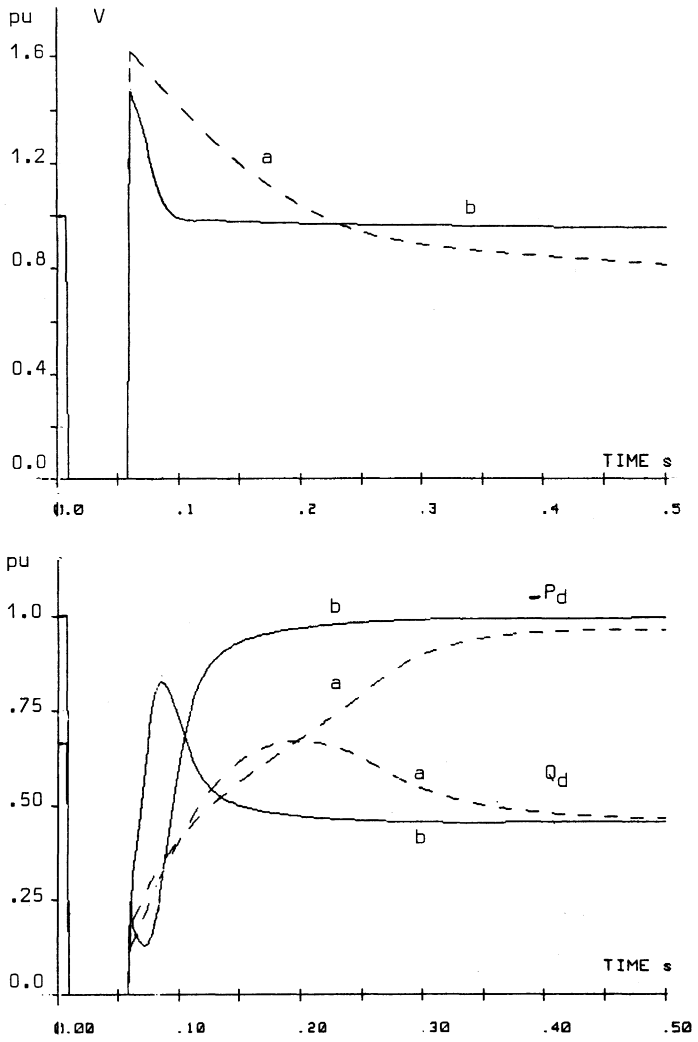

Fig.14 System transient response for a severe ac fault
(a) with conventional converter controls
(b) with new converter controls

A high temporary overvolatge appears after fault clearing with conventional dc converter controls. In this case, the HVDC converter is assumed to be able to deblock against such a high overvoltage. Note that the rate of dc recovery (Pd, Qd) for such a weak ac system condition, is relatively slow. Attempting to reduce the dc recovery time, however, may be unsuccessful as it would lead to a rapid ac voltage collapse and a subsequent commutation failure. Both problems of high temporary overvoltage and voltage instability following dc recovery could be predicted by the VSF in Fig. 4. By the same argument, the small VSF, depicted in Fig. 13 for the new dc controls, imply that the system is free from such problems. This is ultimately evident by the limited temporary overvoltage and the fast and stable recovery performance shown in Fig. 14(b).

CONCLUSIONS

A new simple method for the analysis of ac voltage stability problems at HVDC terminals has been presented. The method can be used to evaluate ac system configurations and VAr compensation schemes before proceeding to other expensive simulation techniques.

A step-by-step technique has been developed for calculating a Voltage Stability Factor for large ac/dc networks with minimum number of computations. Incorporation of the algorithm in available load flow programs has been described.

Examples have been given to show the effects of ac system VAr characteristics, synchronous and static VAr compensators and dc modes of operation on voltage stability for a HVDC scheme connected to weak ac system. Correlation to system dynamic performance has been established.

The application of a new dc control strategy to improve the ac voltage stability under low short circuit ratio conditions have been demonstrated.

REFERENCES

[1] "Overvoltages and Compensation on Integrated AC-DC Systems", Int. Conf., Winnipeg, Canada, July 1980.

[2] A.Gavriolovic, "HVDC Scheme Aspects Influencing the Design of Converter Terminals", Int.Sym. on HVDC Technology, Rio de Janeiro, March 1983.

[3] K.Kanngiesser, W.Kühn, "Tapping of an HVDC Point to Point Transmission as Feed-in to a Relatively weak AC System", CIGRE, SC-14, Rio de Janeiro, July 1981

[4] Y.Yoshide, "Development of a Calculation Method of AC Voltage stability in HVDC Transmission Systems", Electrical Engg. in Japan, 1974, pp.77-85.

[5] A. Hammad, K. Sadek, J. Kauferle, "A New Approach for the Analysis and Solution of ac Voltage Stability Problems at HVDC Terminals", Int. Conf. on DC Power Transmission, June 1984, pp 164-170.

[6] W. Tinney, C. Hart, "Power Flow Solution by Newton's Method", IEEE Trans. Vol. PAS-86, 1967,pp 1449-1460.

[7] P. Dandeno, P. Kundur, "A Non-Iterative Transient Stability Program Including the Effects of Variable Load-Voltage Characteristics", IEEE Trans., Vol. PAS-92, 1973, pp. 1478-1483.

[8] A. Hammad, et.al. ,"Advanced Scheme for AC Voltage Control at HVDC Converter Terminals", IEEE Trans. & Dist. Conf., Kansas City, May '84,paper 84 T&D 385-1

[9] C. Grund, R. Pohl, J. Reeve, "Control Design of an Active and Reactive Power HVDC Modulation System with Kalman Filtering",IEEE Trans.,PAS-101,Oct. 1982

[10] M. Szechtman, W. Ping, E. Salgado, J. Bowles, "Unconventional HVDC Control Techniques for Stabilization of a Weak Power System", IEEE Trans., Vol. PAS-103, Aug. 1984, pp. 2244-2248.

APPENDIX I

Steady State HVDC Terminal Equations

(in pu for both rectifier and inverter)

$Vd = VT \cos\alpha - Rc\ Id$
$Pd = Vd\ Id$
$Qd = Pd \tan\phi$
$Vd = VT \cos\phi$

where;
$Rc = 3Xc/\pi$, T = tap ratio

For inverter : $\cos\gamma = 2\ Rc\ Id/VT - \cos\alpha$